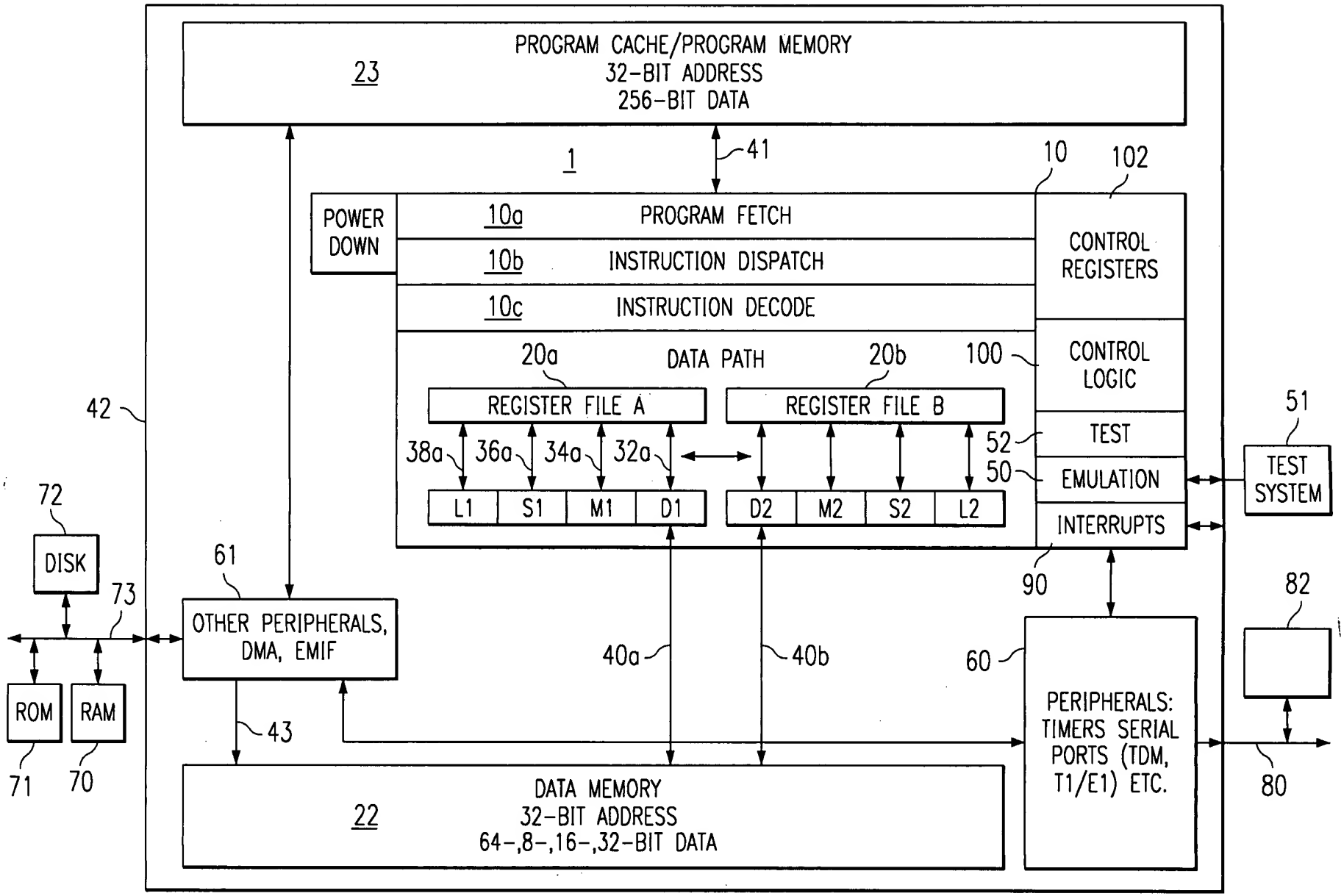
PROGRAM CACHE/PROGRAM MEMORY
32-BIT ADDRESS
256-BIT DATA
23
1
41
10
102
POWER DOWN
10a PROGRAM FETCH
10b INSTRUCTION DISPATCH
10c INSTRUCTION DECODE
CONTROL REGISTERS
20a
DATA PATH
20b
100
CONTROL LOGIC
REGISTER FILE A
REGISTER FILE B
TEST
52
EMULATION
50
INTERRUPTS
38a
36a
34a
32a
L1
S1
M1
D1
D2
M2
S2
L2
42
51
TEST SYSTEM
72
DISK
73
61
OTHER PERIPHERALS, DMA, EMIF
90
82
40a
40b
60
PERIPHERALS: TIMERS SERIAL PORTS (TDM, T1/E1) ETC.
ROM
RAM
71
70
43
80
DATA MEMORY
32-BIT ADDRESS
64-,8-,16-,32-BIT DATA
22

*FIG. 1*

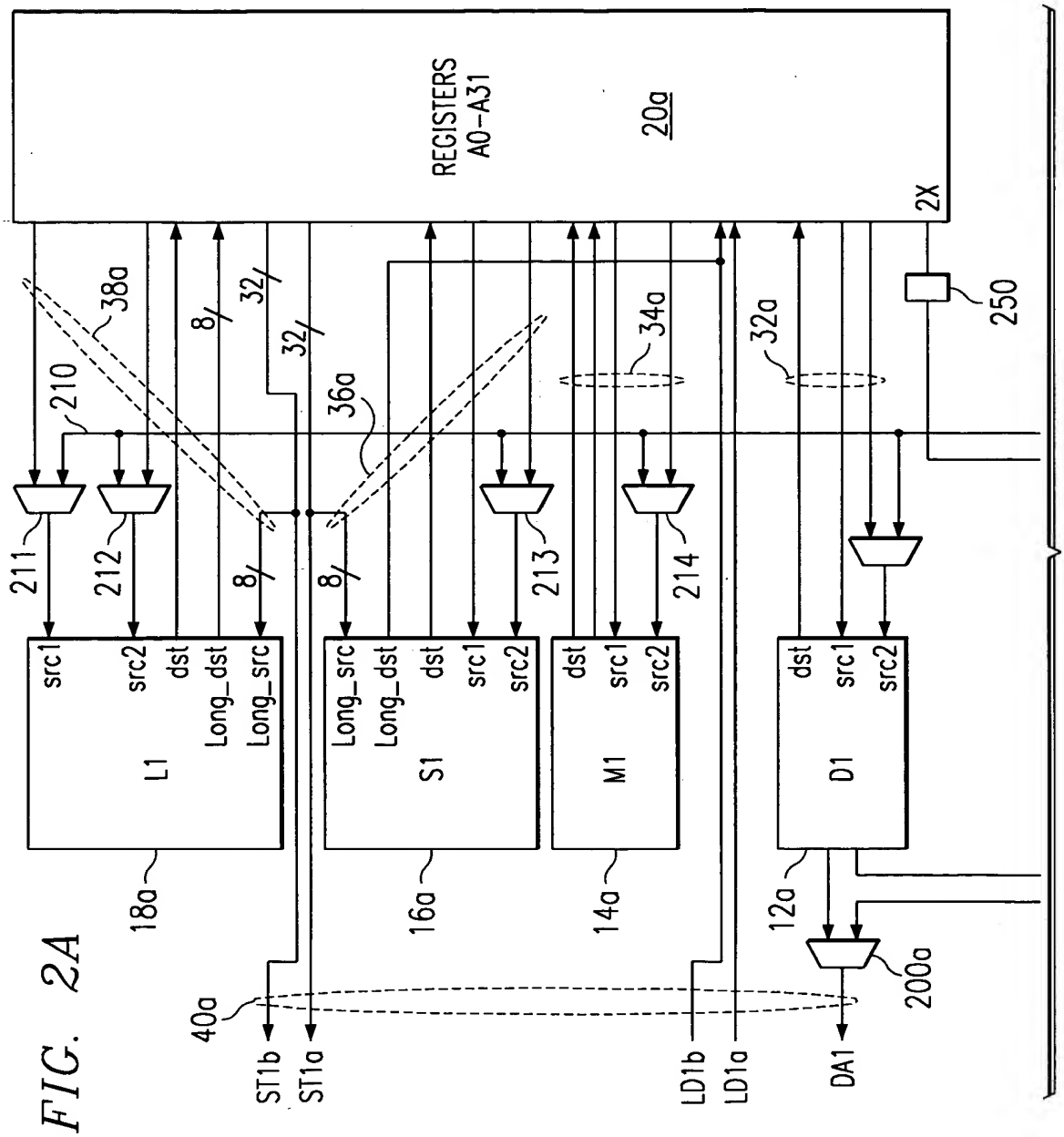
REGISTERS
A0-A31
20a
2X
250
38a
32
8
32
36a
34a
32a
210
211
212
213
214
8
8
src1
src2
dst
Long_dst
Long_src
L1
18a
Long_src
Long_dst
dst
src1
src2
S1
16a
dst
src1
src2
M1
14a
dst
src1
src2
D1
12a
200a
40a
ST1b
ST1a
LD1b
LD1a
DA1
TO FIG. 2B

FIG. 2A

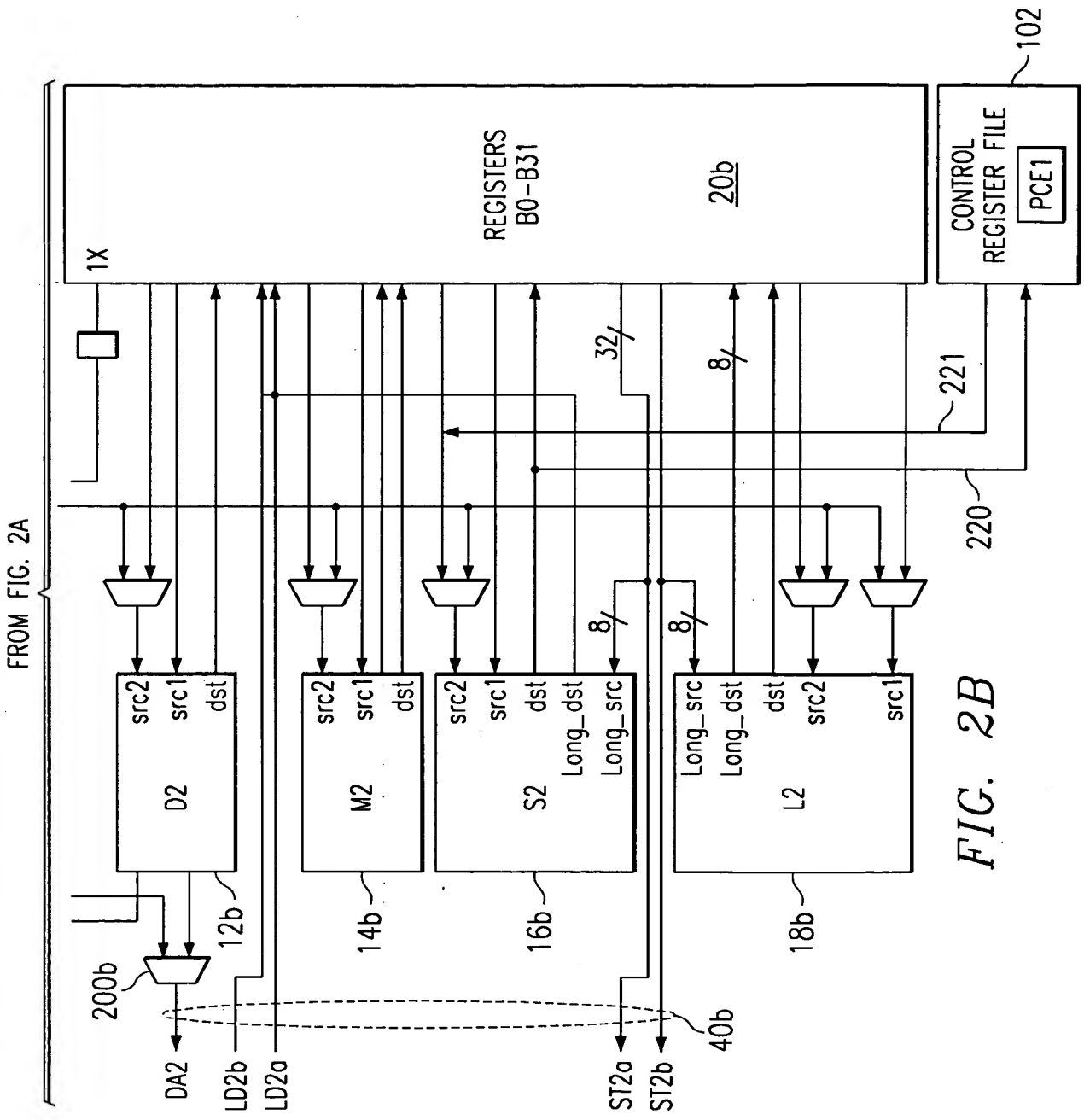
FROM FIG. 2A
1X
REGISTERS B0-B31
20b
CONTROL REGISTER FILE
PCE1
102
221
220
32
8
D2
src2
src1
dst
12b
M2
14b
S2
Long_dst
Long_src
16b
L2
18b
200b
40b
DA2
LD2b
LD2a
ST2a
ST2b

FIG. 2B

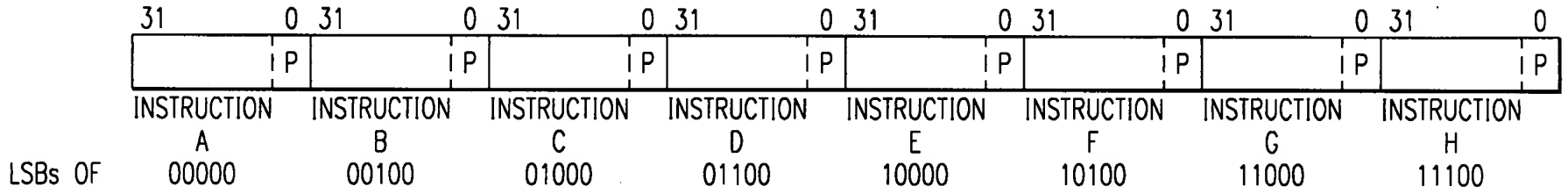


FIG. 3A

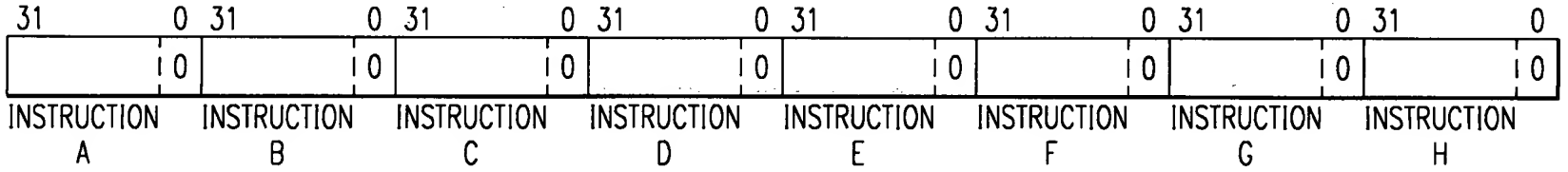


FIG. 3B

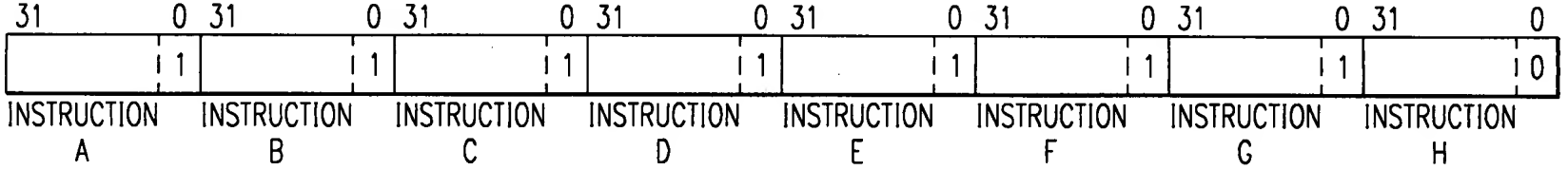


FIG. 3C

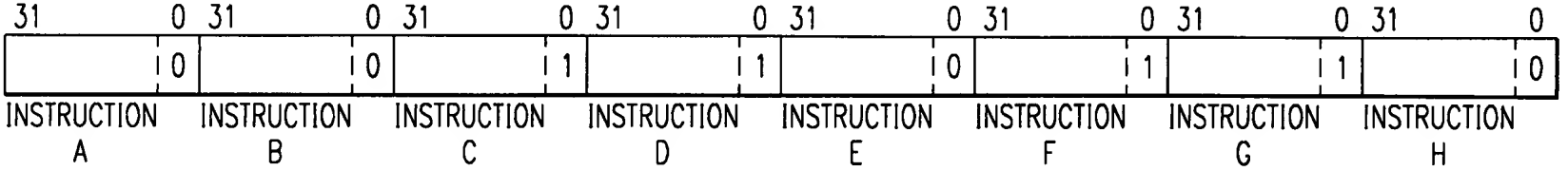


FIG. 3D

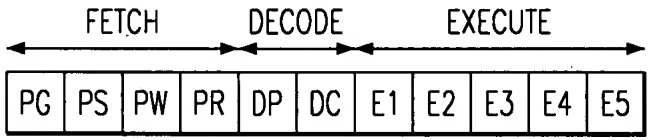


FIG. 4A

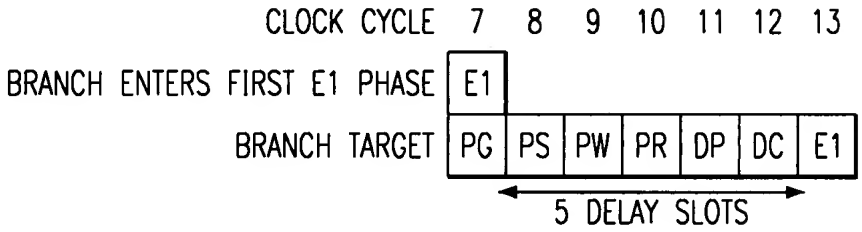


FIG. 4B

| FETCH PACKET | EXECUTE PACKET | CLOCK CYCLE 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| n | k | PG | PS | PW | PR | DP | DC | E1 | E2 | E3 | E4 | E5 | | | | | | | | | | | | |
| n | k+1 | | | | | | DP | DC | E1 | E2 | E3 | E4 | E5 | | | | | | | | | | | |
| n | k+2 | | | | | | | DP | DC | E1 | E2 | E3 | E4 | E5 | | | | | | | | | | |
| n+1 | k+3 | | PG | PS | PW | PR | PR | PR | DP | DC | E1 | E2 | E3 | E4 | E5 | | | | | | | | | |
| n+2 | k+4 | | | PG | PS | PW | PW | PW | PR | DP | DC | E1 | E2 | E3 | E4 | E5 | | | | | | | | |
| n+3 | k+5 | | | | PG | PS | PS | PS | PW | PR | DP | DC | E1 | E2 | E3 | E4 | E5 | | | | | | | |
| n+4 | k+6 | | | | | PG | PG | PG | PS | PW | PR | DP | DC | E1 | E2 | E3 | E4 | E5 | | | | | | |
| n+5 | k+7 | | | | | | | | PG | PS | PW | PR | DP | DC | E1 | E2 | E3 | E4 | E5 | | | | | |
| n+6 | k+8 | | | | | | | | | PG | PS | PW | PR | DP | DC | E1 | E2 | E3 | E4 | E5 | | | | |

FIG. 4C

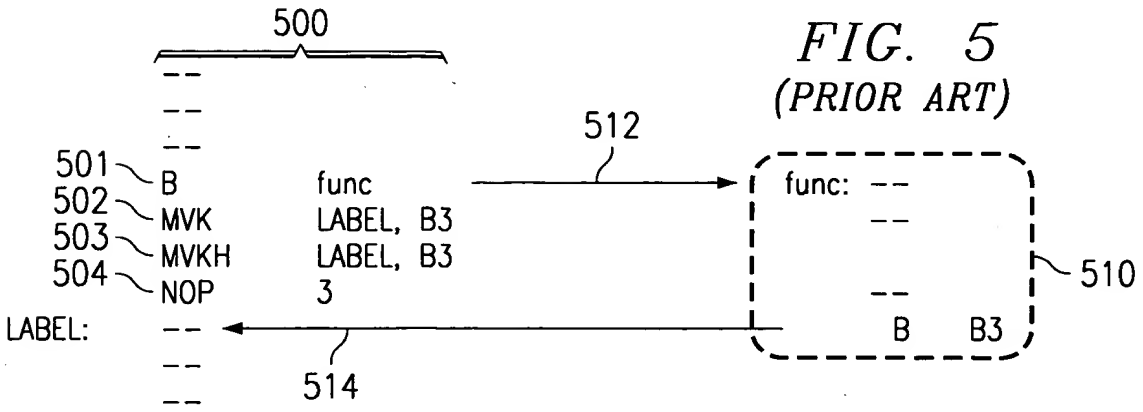


FIG. 5
(PRIOR ART)

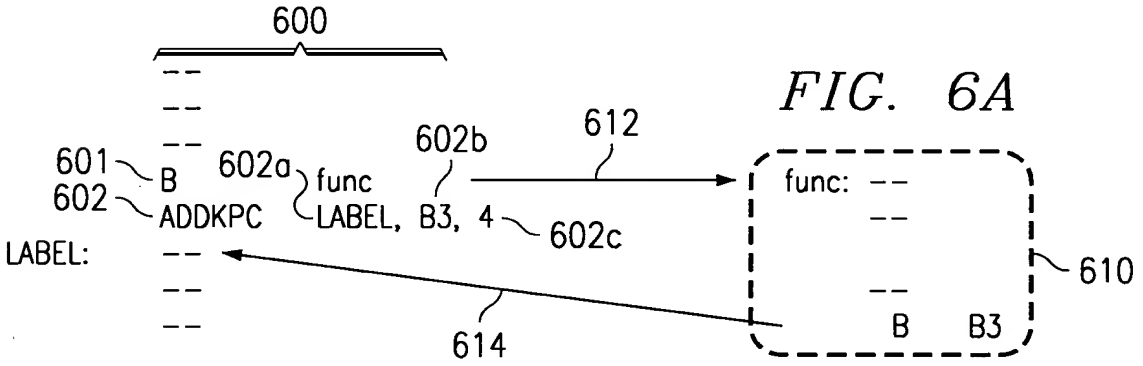


FIG. 6A

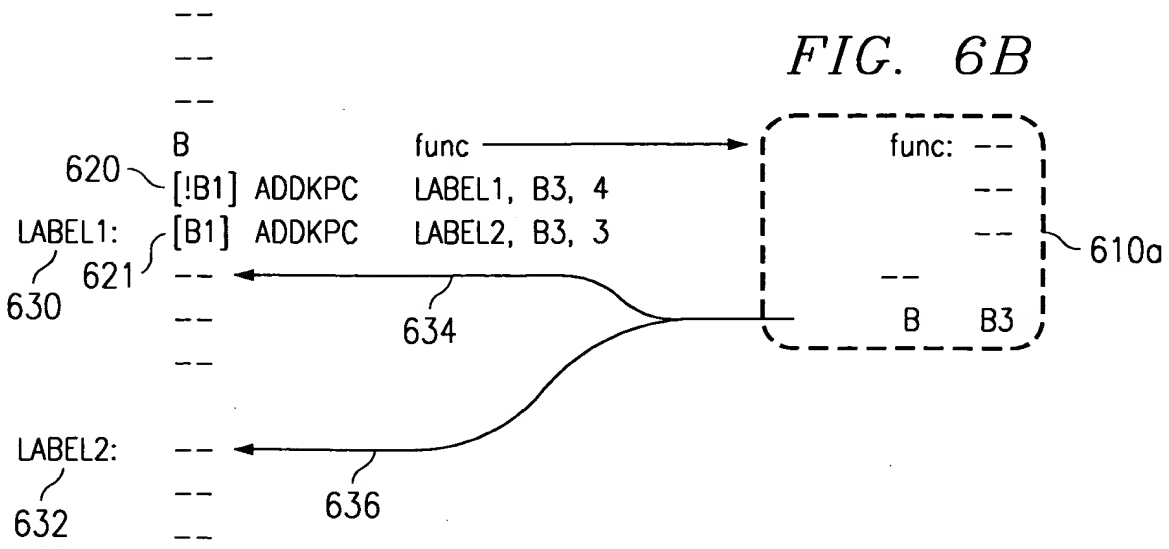


FIG. 6B

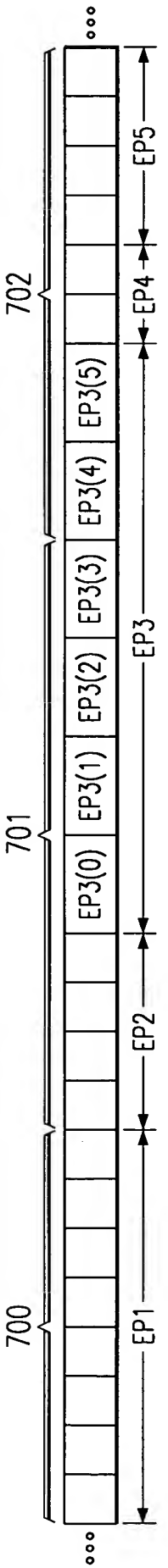
700
701
702
EP1
EP2
EP3
EP4
EP5
EP3(0)
EP3(1)
EP3(2)
EP3(3)
EP3(4)
EP3(5)

FIG. 7

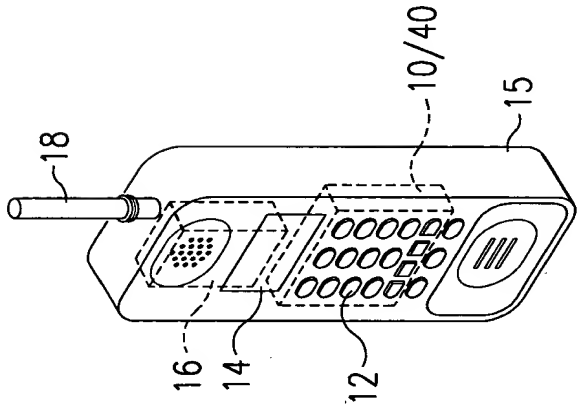
18
10/40
15
16
14
12

FIG. 11

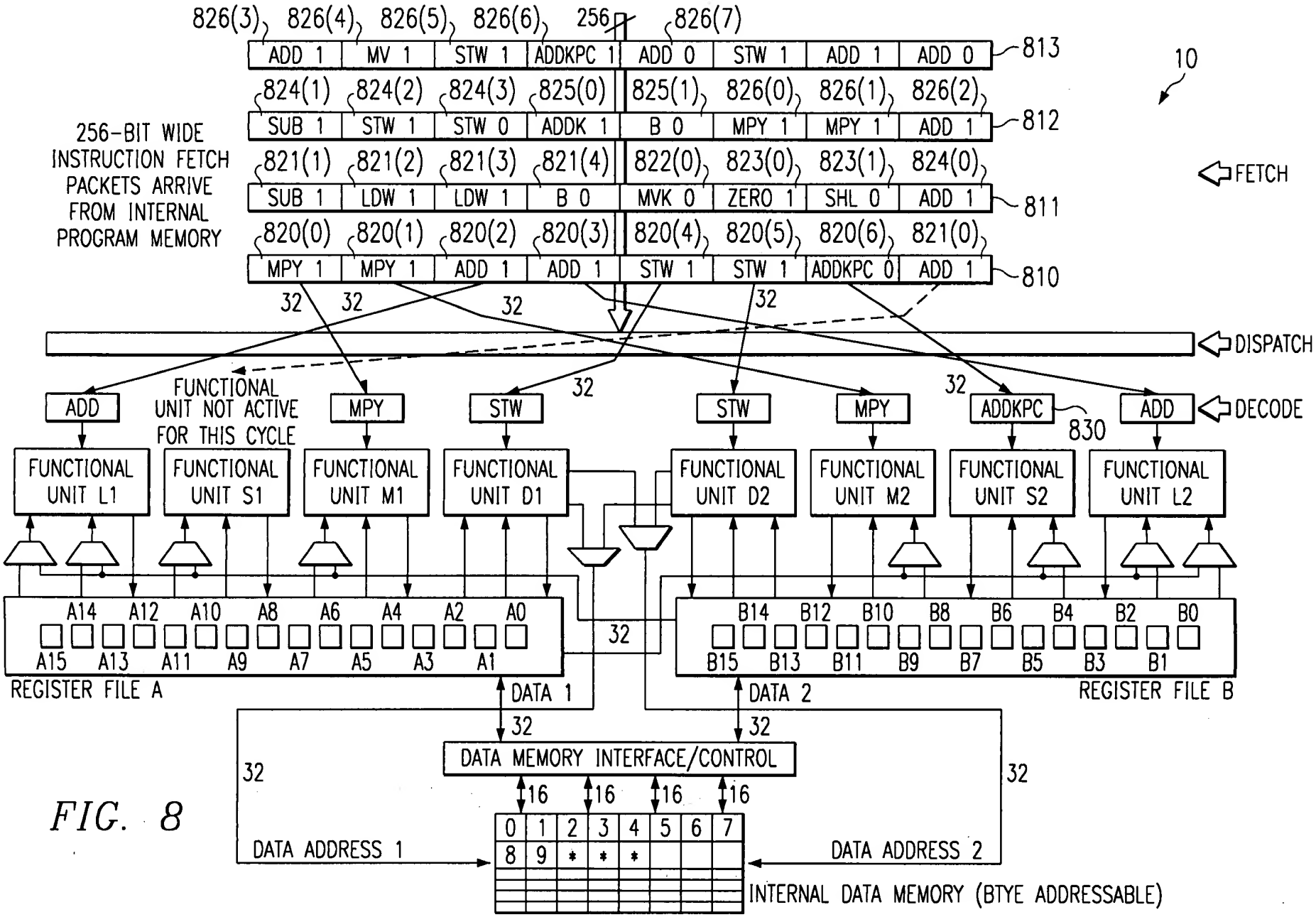
826(3) 826(4) 826(5) 826(6) 256 826(7)
ADD 1 | MV 1 | STW 1 | ADDKPC 1 | ADD 0 | STW 1 | ADD 1 | ADD 0
813
10
824(1) 824(2) 824(3) 825(0) 825(1) 826(0) 826(1) 826(2)
SUB 1 | STW 1 | STW 0 | ADDK 1 | B 0 | MPY 1 | MPY 1 | ADD 1
812
256-BIT WIDE INSTRUCTION FETCH PACKETS ARRIVE FROM INTERNAL PROGRAM MEMORY
821(1) 821(2) 821(3) 821(4) 822(0) 823(0) 823(1) 824(0)
SUB 1 | LDW 1 | LDW 1 | B 0 | MVK 0 | ZERO 1 | SHL 0 | ADD 1
811
FETCH
820(0) 820(1) 820(2) 820(3) 820(4) 820(5) 820(6) 821(0)
MPY 1 | MPY 1 | ADD 1 | ADD 1 | STW 1 | STW 1 | ADDKPC 0 | ADD 1
810
32 32 32 32
DISPATCH
ADD
FUNCTIONAL UNIT NOT ACTIVE FOR THIS CYCLE
MPY
STW
32
STW
MPY
32
ADDKPC
830
ADD
DECODE
FUNCTIONAL UNIT L1
FUNCTIONAL UNIT S1
FUNCTIONAL UNIT M1
FUNCTIONAL UNIT D1
FUNCTIONAL UNIT D2
FUNCTIONAL UNIT M2
FUNCTIONAL UNIT S2
FUNCTIONAL UNIT L2
A14 A12 A10 A8 A6 A4 A2 A0
A15 A13 A11 A9 A7 A5 A3 A1
32
B14 B12 B10 B8 B6 B4 B2 B0
B15 B13 B11 B9 B7 B5 B3 B1
REGISTER FILE A
DATA 1
DATA 2
REGISTER FILE B
32
32
32
DATA MEMORY INTERFACE/CONTROL
32
16 16 16 16
0 1 2 3 4 5 6 7
8 9 * * *
DATA ADDRESS 1
DATA ADDRESS 2
INTERNAL DATA MEMORY (BTYE ADDRESSABLE)

*FIG. 8*

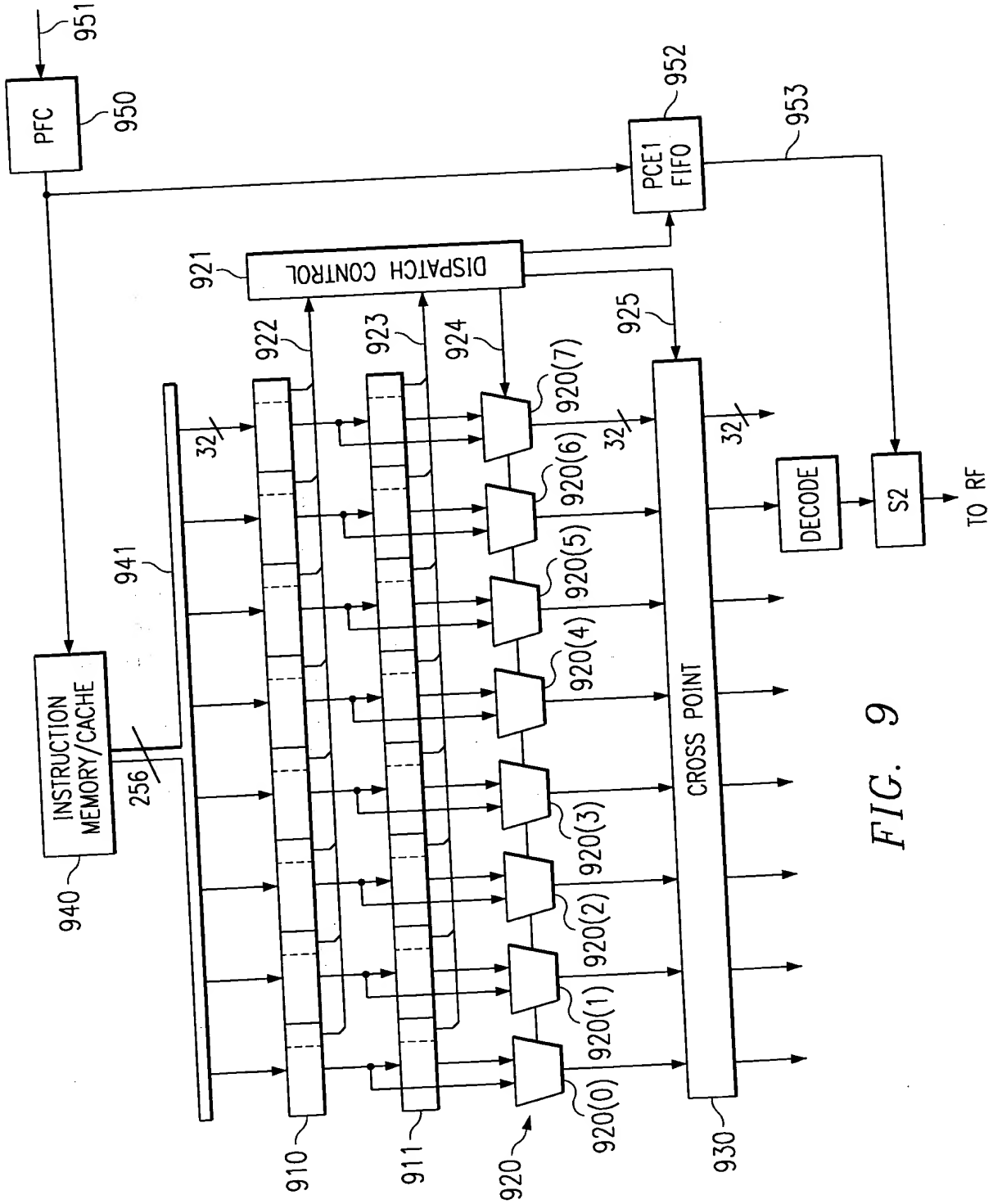
951
PFC
950
952
PCE1 FIFO
953
921
DISPATCH CONTROL
922
923
924
925
941
INSTRUCTION MEMORY/CACHE
256
940
32
920(7)
920(6)
920(5)
920(4)
920(3)
920(2)
920(1)
920(0)
CROSS POINT
DECODE
S2
TO RF
910
911
920
930

FIG. 9

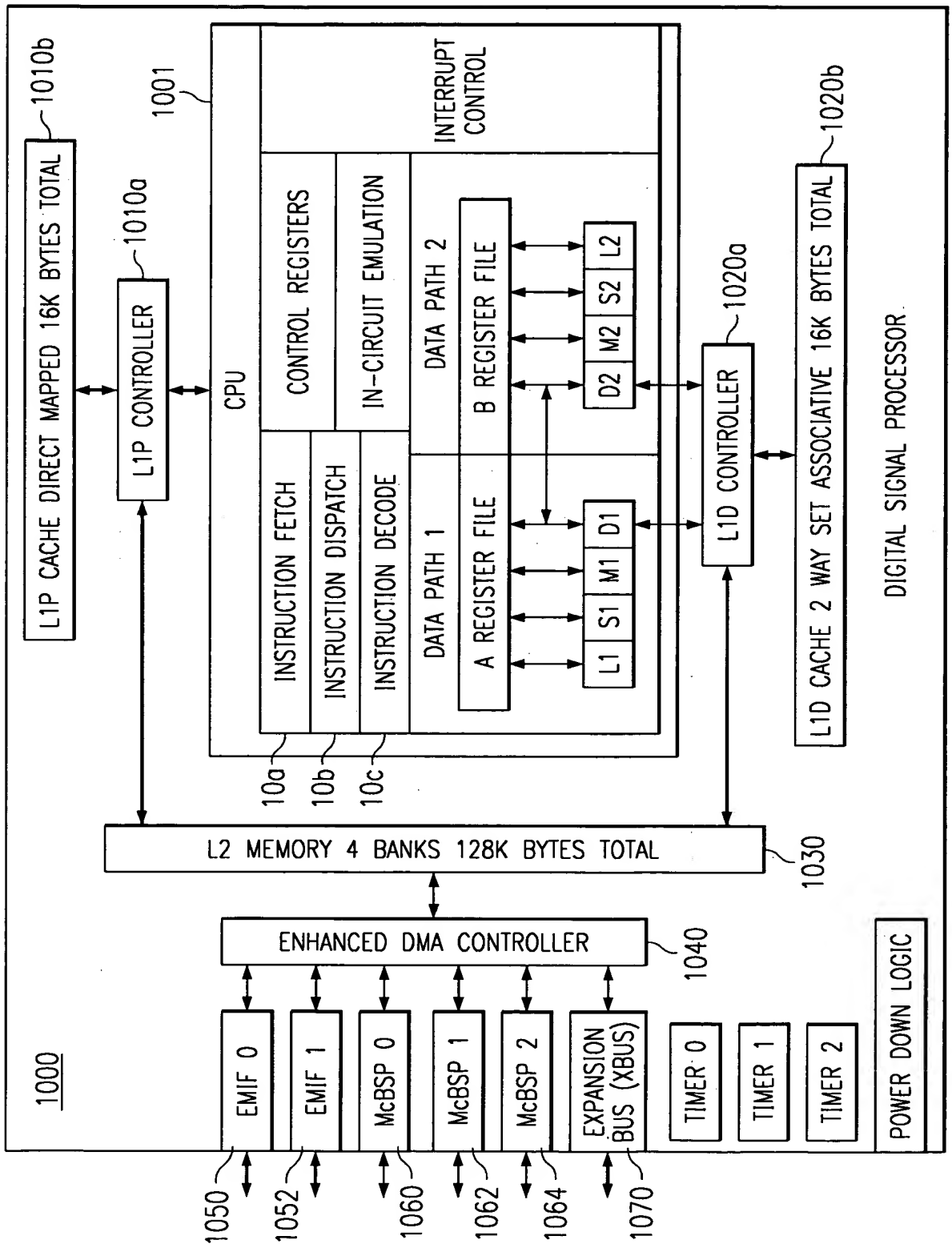
1000
L1P CACHE DIRECT MAPPED 16K BYTES TOTAL
1010b
L1P CONTROLLER
1010a
1001
CPU
INSTRUCTION FETCH
INSTRUCTION DISPATCH
INSTRUCTION DECODE
CONTROL REGISTERS
IN-CIRCUIT EMULATION
INTERRUPT CONTROL
DATA PATH 1
A REGISTER FILE
L1
S1
M1
D1
DATA PATH 2
B REGISTER FILE
D2
M2
S2
L2
10a
10b
10c
L1D CONTROLLER
1020a
L1D CACHE 2 WAY SET ASSOCIATIVE 16K BYTES TOTAL
1020b
DIGITAL SIGNAL PROCESSOR
L2 MEMORY 4 BANKS 128K BYTES TOTAL
1030
ENHANCED DMA CONTROLLER
1040
EMIF 0
EMIF 1
McBSP 0
McBSP 1
McBSP 2
EXPANSION BUS (XBUS)
TIMER 0
TIMER 1
TIMER 2
POWER DOWN LOGIC
1050
1052
1060
1062
1064
1070

FIG. 10